

ABSTRACT

Resistance and capacitance are added to a prototype die to fix or identify performance issues with the integrated circuit formed in the die

5 by forming a thin piece of silicon on the top surface of the die. For resistance, vias are formed to regions on the metal traces and to opposite ends of the piece of silicon using a FIB system. For capacitance, a dielectric is formed on the piece of silicon, and a layer of metal is formed on the dielectric. Vias are formed to regions on the

10 metal traces, to the piece of silicon, and to the layer of metal using the FIB system.